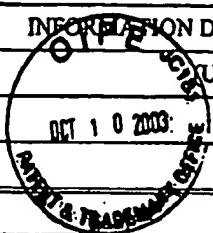


U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.		
				01N006-1C US		09/849,005		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicants: Chian-Min Ho et al.				
				Filing Date		Group 2128		
				MAY 4, 2001		2123		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
RF	AA	5,555,270	9/10/96	Sun et al.	371	27	/	
RF	AB	5,630,051	5/13/97	Sun et al.	395	183.08		
RF	AC	5,600,787	2/4/97	Underwood et al.	395	183.06		
RF	AD	5,623,499	4/22/97	Ko et al.	371	22.1		
RF	AE	5,654,657	8/5/97	Pearce	327	163		
RF	AF	5,729,554	3/17/98	Weir et al.	371	27		
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	Windley, Phillip J., "Formal Modeling and Verification of Microprocessors", IEEE Transactions on Computers, Vol. 44, No. 1, January 1995, pp. 54-72.						
RF	AJ	Clarke, E. M., et al., "Efficient Generation of Counterexamples and Witnesses in Symbolic Model Checking", 32 <sup>nd</sup> Design Automation Conference, June 12-16, 1995, pp. 427-432.						
RF	AK	Silburt, Allan, et al., "Accelerating Concurrent Hardware Design with Behavioral Modelling and System Simulation", 32 <sup>nd</sup> Design Automation Conference, June 12-16, 1995, pp. 528-533.						
RF	AL	Jones, Robert B., et al., "Efficient Validity Checking for Processor Verification", IEEE International Conference on Computer-Aided Design, November 5-9, 1995, pp. 2-6.						
RF	AM	Clarke, Edmund M., et al., "Model Checking and Abstraction", ACM Press Conference Record of the Nineteenth Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, January 19-22, 1992, pp. 343-354.						
RF	AN	Aagaard, Mark D., et al., "The Formal Verification of a Pipelined Double-Precision IEEE Floating-Point Multiplier", 1995 IEEE/ACM International Conference on Computer-Aided Design, November 5-9, 1995, pp. 7-10.						
RF	AO	Clarke, E. M., "Representing Circuits More Efficiently in Symbolic Model Checking", 28 <sup>th</sup> ACM/IEEE Design Automation Conference, June 17-21, 1991, pp. 403-407.						
Examiner		Russell Fred		Date Considered		1.12.05		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
				01N008-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		2128	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes N
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Bombana, M., et al., "Design-Flow and Synthesis for ASICs: a case study", 32 <sup>nd</sup> Design Automation Conference, June 12-16, 1995, pp. 292-297.					
RF	AJ	Beer, Ilan, et al., "Methodology and System for Practical Formal Verification of Reactive Hardware", 6 <sup>th</sup> International Conference, CAV '94, June 21-23, 1994, Proceedings, pp. 183-193.					
RF	AK	Daga, A., "A Symbolic-Simulation Approach to the Timing Verification of Interacting FSMs", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, 584-589.					
RF	AL	Matsunaga, Y., "An Efficient Equivalence Checker for Combinational Circuits", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996 Proceedings, pp. 629-634.					
RF	AM	Balarin, F., et al., "Formal Verification of Embedded Systems based on CFSM Networks", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, 568-571.					
RF	AN	Stornetta, T., et al., "Implementation of an Efficient Parallel BDD Package", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, 641-644.					
RF	AO	<a href="http://www.pure.com">http://www.pure.com</a> , Purify User's Guide, Version 4.0, believed to be prior to October 1997.					
Examiner		Russell FRETD		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.		
				01N006-1C US		09/849,005		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.				
(Use several sheets if necessary)								
				Filing Date		Group 2128		
				MAY 4, 2001		2128		
U.S. Patent Documents								
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
	Document	Date	Country	Class	Subclass	Yes	No	
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	DeMillo, Richard A., et al., "Software Testing and Evaluation", Software Engineering Research Center, Georgia Institute of Technology, 1997.						
RF	AJ	Groz, R., et al. "Attacking A Complex Distributed Algorithm from Different Sides: An Experience with Complementary Validation Tools", Proc. IFIP WG 6.1 Fourth International Workshop on Protocol Specification, Testing and Verification, Skytop Lodge, Pennsylvania, June 1984, pp. 315-331.						
RF	AK	Nurie, G. "Attain Testability With Hierarchical Design", Electronic Design, June 27, 1991, pp. 89-99.						
RF	AL	Blum, M., et al., "Software Reliability via Run-Time Result-Checking", Proc. 35 <sup>th</sup> IEEE FOCS, 1994.						
RF	AM	Ho, Chian-Min Richard, "Validation Tools For Complex Digital Designs", A Dissertation Submitted to the Department of Computer Science and the Committee on Graduate Studies of Stanford University in Partial Fulfillment of the Requirements For the Degree of Doctor of Philosophy, November 1996.						
RF	AN	Von Bochmann, G., "Concepts for Distributed Design", Springer-Verlag Berlin Heidelberg New York, 1983.						
RF	AO	Torku, K. E., "Fault Test Generation for Sequential Circuits: A Search Directing Heuristic", Ph.D. Thesis, University of Oklahoma, 1979.						
Examiner		Date Considered						
RUSSELL FREED		1.12.05						
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				OIN006-IC US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicants: Chian-Min Ho et al.			
				Filing Date		Group 2128	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Belt, J. E., "An Heuristic Search Approach to Test Sequence Generation for AHPL Described Synchronous Sequential Circuits", Ph.D. Thesis, University of Arizona, 1973.					
RF	AJ	http://www.parasoft.com, "Insure++ Getting Started Version 3.0.1", believed to be prior to October 1997..					
RF	AK	Huey, B. M., "Search Directing Heuristics for the Sequential Circuit Test Search System (SCIRTSS)", Ph.D. Thesis, University of Arizona, 1975.					
RF	AL	Deutsch, M. S., "Software Verification and Validation", Prentice-Hall, Englewood Cliffs, NJ, 1982.					
RF	AM	Masud, M., et al., "Functional Test Using Behavior Models", Digest of Papers COMPCON Spring 1992, San Francisco, CA February 1992, pp. 446-451.					
RF	AN	Brayton, R. K., et al., "VIS" First International Conference Formal Methods in Computer Aided Design, FMCAD'96, Palo Alto, CA, November 1996, pp. 248-256.					
RF	AO	Chandra, A. K., et al., "Architectural Verification of Processors Using Symbolic Instruction Graphs", Computer Science, February 9, 1994, pp. 1-23.					
Examiner		Russell Fred		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

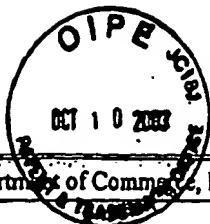
U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						OIN006-1C US		09/849,005	
						Applicants: Chian-Min Ho et al.			
						Filing Date		Group 2/28	
						MAY 4, 2001		2123	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Burch, Jerry R., et al., "Automatic Verification of Pipelined Microprocessor Control", Computer Aided Verification, 6 <sup>th</sup> International Conference, CAV'94, Stanford, CA, June 21-23, 1994 Proceedings, pp. 69-80.							
RF	AJ	Malley, Charles, et al., "Logic Verification Methodology for Power PC <sup>TM</sup> Microprocessors", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 234-240.							
RF	AK	Campos, S., et al., "Verifying the Performance of the PCI Local Bus using Symbolic Techniques", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, Austin, Texas, pp. 72-78.							
RF	AL	<a href="http://www.synopsys.com/pubs/JHLD/JHLD-099402">http://www.synopsys.com/pubs/JHLD/JHLD-099402</a> , System Design and Validation, believed to be prior to October 1997.							
RF	AM	Beatty, Derek L., "Formally verifying a microprocessor using a simulation methodology", 31 <sup>st</sup> Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 596-602.							
RF	AN	Beer, Ilan, et al., "Rule-Base: an Industry-Oriented Formal Verification Tool", 33 <sup>rd</sup> Design Automation Conference, Proceedings 1996, 655-660.							
RF	AO	Bormann, Jorg, et al., "Model Checking in Industrial Hardware Design", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 298-303.							
Examiner		Russell FREED		Date Considered		1.12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

PART "B"

Sheet 6 of 24

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Hoskote, Y. V., et al., "Automatic Extraction of the Control Flow Machine and Application to Evaluating Coverage of Verification Vectors", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, pp. 532-537.					
RF	AJ	Mihail, Milena, et al., "On the Random Walk Method for Protocol Testing", Computer Aided Verification, 6 <sup>th</sup> International Conference, CAV '94, Stanford, CA, June 21-23, 1994, pp. 133-141.					
RF	AK	Cheng, Kwang-Ting, "Automatic Generation of Functional Vectors Using the Extended Finite State Machine Model", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 57-78.					
RF	AL	Ramalingam, T., et al., "On conformance test and fault resolution of protocols based on FSM model", Proceedings of the IFIP TC6 Working Conference on Computer Networks, Architecture and Applications, NETWORKS '92, Trivandrum, India October 28-29, 1992, pp. 211-223.					
RF	AM	Chechik, M., et al., "Automatic Verification of Requirements Implementation", Proc. 1994 International Symposium on Software Testing and Analysis (ISSTA), Seattle, WA, August 1994, pp. 109-124.					
RF	AN	v. Bochmann, G. et al., "Protocol Testing: Review of Methods and Relevance for Software Testing", ACM Press, Proceedings of the 1994 International Symposium on Software Testing and Analysis (ISSTA), Seattle, Washington, August 17-19, 1994.					
RF	AO	Fujiwara, S., et al., "Test Selection Based on Finite State Models", IEEE Transactions on Software Engineering, Vol. 17, No. 6, June 1991, pp. 591-603.					
Examiner		RUSSELL FERTD		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.	
				01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AJ	Forghani, B. et al., "Semi-automatic test suite generation from Estelle", Software Engineering Journal, July 1992, pp. 295-307.					
RF	AJ	Fuchs, N. E., "Specifications are (preferably) executable", Software Engineering Journal, September 1992, pp. 323-334.					
RF	AK	Narasimhan, Naren, et al., "Specification of Control Flow Properties for Verification of Synthesized VHDL Designs", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 326-345.					
RF	AL	Keutzer, K., "The Need for Formal Verification in Hardware Design and What Formal Verification Has Not Done for Me Lately", Workshop on the HOL Theorem Proving System and its Application, 1991, pp. 77-86.					
RF	AM	Eiriksson, Asgeir T., "Integrating Formal Verification Methods with A Conventional Project Design Flow", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 666-671.					
RF	AN	Borrione, D., et al., "HDL-Based Integration of Formal Methods and CAD Tools in the PREVAIL Environment", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 451-467.					
RF	AO	Aziz, A., et al., "HSIS: A BDD-Based Environment for Formal Verification", 31 <sup>st</sup> Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 454-459.					
Examiner		RUSSELL FREED		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							



PART "B"

Sheet 8 of 24

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
						01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)									
						Filing Date		Group 2128	
						MAY 4, 2001		2123	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Behcet, S., et al., "A Test Design Methodology for Protocol Testing", IEEE Transactions on Software Engineering, Vol. SE-13, No. 5, May 1987, pp. 518-531.							
RF	AJ	v. Bochman, G., "Usage of Protocol Development Tools: The Results of a Survey", Protocol IFIP WG 6.1, Seventh International Workshop on Protocol Specification, Testing and Verification, 1987, pp. 139-161.							
RF	AK	Borgmann, J., et al., "Model Checking in Industrial Hardware Design", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 298-303.							
RF	AL	Miczo, A., "Digital Logic Testing and Simulation", John Wiley & Sons, New York, NY, 1986.							
RF	AM	Naik, V. G., et al., "Modeling and Verification of a Real Life Protocol Using Symbolic Model Checking", Computer Aided Verification, 6 <sup>th</sup> International Conference, CAV '94, Stanford, CA June 21-23, 1994, pp. 195-206.							
RF	AN	Smith, S., et al., "Demand Driven Simulation: BACKSIM", 24 <sup>th</sup> ACM/IEEE Design Automation Conference, Proceedings 1987, pp. 181-187.							
RF	AO	Levitt, J., et al., "A Scalable Format Verification Methodology for Pipelined Microprocessors", 33 <sup>rd</sup> Design Automation Conference, Proceedings 1996, pp. 558-563.							
Examiner		RUSSELL FREED		Date Considered		1.12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									



PART "B"

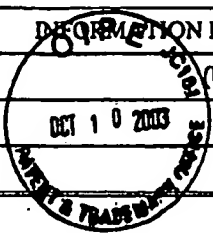
Sheet 9 of 24

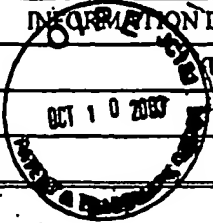
U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
				OIN 006-1 C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Burch, J. R., "Techniques for Verifying Superscalar Microprocessors", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 552-557.					
RF	AJ	Jones, K. D., et al., "The Automatic Generation of Functional Test Vectors for Rambus Designs", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 415-420.					
RF	AK	Nelson, B. E., et al., "Simulation Event Pattern Checking with PROTO", June 14, 1993.					
RF	AL	Fallah, F., et al., "Functional Vector Generation for HDL models Using Linear Programming and 3-Satisfiability, believed to be prior to October 1997.					
RF	AM	Moundanos, D., "Abstraction Techniques for Validation Coverage Analysis and Test Generation", IEEE Transactions on Computers, Vol. 47, January 1998, pp. 2-14.					
RF	AN	Hsiao, M. S., et al., "Application of Genetically Engineered Finite-State-Machine Sequences to Sequential Circuit ATPG", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 3, March 1998, pp. 239-254.					
RF	AO	Gregory, B., et al., "Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof", <a href="http://patent.wompi.net/number=5661661">http://patent.wompi.net/number=5661661</a> , believed to be prior to October 1997.					
Examiner		RUSSELL FRETZ		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
				01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicants: Chian-Min Ho et al.			
				Filing Date		Group 2128	
				MAY 4, 2001		2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Hastings, R., "Method for inserting new machine instructions into preexisting machine code to monitor preexisting machine access to memory", <a href="http://patent.womp...ent_number=5335344">http://patent.womp...ent_number=5335344</a> , believed to be prior to October 1997.					
RF	AJ	Hastings, R., "Method and apparatus for modifying relocatable object code files and monitoring programs", <a href="http://patent.womp...ent_number=5335329">http://patent.womp...ent_number=5335329</a> , believed to be prior to October 1997.					
RF	AK	Cheng, K. T., "Automatic Functional Test Generation Using The Extended Finite State Machine Model", 30 <sup>th</sup> Design Automation Conference, Dallas, Texas, June 14-18, Proceedings 1993, pp. 86-91.					
RF	AL	Burch, J. R., et al., "Symbolic Model Checking: 10 <sup>20</sup> States and Beyond", Information and Computation, 1998, pp. 142-170.					
RF	AM	Keutzer, K., "The Need for Formal Methods for Integrated Circuit Design", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 1-19.					
RF	AN	Devadas, S., et al., "An Observability-Based Code Coverage Metric for Functional Simulation", IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 1996, pp. 418-425.					
RF	AO	Lewin, D., et al., "A Methodology for Processor Implementation Verification", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 126-143.					
Examiner		RUSSELL FRED		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

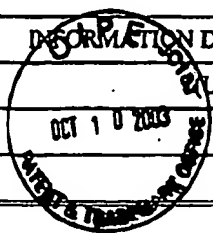
U.S. Department of Commerce, Patent and Trademark Office						Atty. Docket No.		Serial No.	
						01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)									
						Filing Date		Group	
						MAY 4, 2001		2123	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Aharon, A., et al., "Test Program Generation for Functional Verification of PowerPC Processors in IBM", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 279-285.							
RF	AJ	Santucci, J., et al., "Speed up of Behavioral A.T.P.G. Using a Heuristic Criterion", 30 <sup>th</sup> Design Automation Conference, Dallas, Texas, June 14-18, 1993, pp. 92-96.							
RF	AK	Abadir, M., et al., "Logic Design Verification via Test Generation", IEEE Transactions on Computer-Aided Design, Vol. 7, No. 1, January 1988, pp. 138-148.							
RF	AL	Schlipf, T., et al., "Formal verification made easy", <a href="http://www.almaden...d/414/schlipf.html">http://www.almaden...d/414/schlipf.html</a> , believed to be prior to October 1997.							
RF	AM	Moore, J. S., "Introduction to the OBDD Algorithm for the ATP Community", Technical Report 84, October 1992.							
RF	AN	Bryant, R. E., "Binary Decision Diagrams and Beyond: Enabling Technologies for Formal Verification", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 5-9, 1995, pp. 236-243.							
RF	AO	Hoskote, Y. V., et al., "Automatic Verification of Implementations of Large Circuits Against HDL Specifications", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 3, March 1997, pp. 217-228.							
Examiner		RUSSELL FRETZ		Date Considered		1.12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.		
				OJN006-1C US		09/849,005		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.				
(Use several sheets if necessary)								
				Filing Date		Group		
				MAY 4, 2001		2128		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	Goel, P., "An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits", IEEE Transactions on Computers, Vol. C-30, No. 3, March 1981, pp. 215-222.						
RF	AJ	Jones, R., et al., "Self-Consistency Checking", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 158-171.						
RF	AK	Sajkowski, M., "Protocol Verification Techniques: Status Quo and Perspectives", Proc. IFIP WG 6.1 Fourth International Workshop on Protocol Specification, Testing and Verification, Skytop Lodge, Pennsylvania, June 1984, pp. 697-720.						
RF	AL	McMillan, K. L., "Fitting Formal Methods into the Design Cycle", 31 <sup>st</sup> Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 314-319.						
RF	AM	Geist, D., et al., "Coverage-Directed Test Generation Using Symbolic Techniques", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 142-159.						
RF	AN	Motohara, A., et al., "A State Traversal Algorithm Using a State Covariance Matrix", 30 <sup>th</sup> Design Automation Conference, Dallas, Texas, June 14-18, 1993, pp. 97-101.						
RF	AO	Bryant, R. E., et al., "Formal Hardware Verification by Symbolic Ternary Trajectory Evaluation", 28 <sup>th</sup> ACM/IEEE Design Automation Conference, San Francisco, CA, June 17-21, 1991, pp. 397-402.						
Examiner		RUSSELL FRETZ		Date Considered		1.12.05		
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

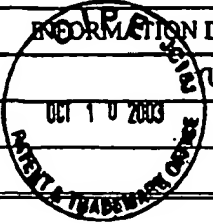
U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				QINOC6-ICUS		09/849,005		
				Applicants: Chian-Min Ho et al.				
				Filing Date		Group 2128		
				MAY 4, 2001		2123		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	Coudert, O., et al., "Verification of Synchronous Sequential Machines Based on Symbolic Execution", Automatic Verification Methods for Finite State Systems, International Workshop, Grenoble, France, June 12-14, 1989, pp. 365-373.						
RF	AJ	Sangiovanni-Vincentelli, A., "Verification of Electronic Systems", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 106-111.						
RF	AK	Chandra, A. K., et al., "Constraint Solving for Test Case Generation", IEEE International Conference on Computer Design, 1992, pp. 245-248.						
RF	AL	Chung, Pi-Yu, "Diagnosis and Correction of Logic Design Errors in Digital Circuits", 30 <sup>th</sup> Design Automation Conference, Dallas, Texas, June 14-18, 1993, pp. 503-508.						
RF	AM	Chandra, A. K., "Architectural Verification of Processors Using Symbolic Instruction Graphs", IEEE International Conference on Computer Design, 1994, pp. 454-459.						
RF	AN	Hastings, R., "System for modifying relocatable object code files to monitor accesses to dynamically allocated memory"; <a href="http://patent.womp...ent_number=5193180">http://patent.womp...ent_number=5193180</a> , believed to be prior to October 1997.						
RF	AO	Gately, J., "Verifying a Million-Gate Processor", Integrated System Design, October 1997, pp. 19-23.						
Examiner		RUSSELL FREED		Date Considered				1.12.05
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.		
				OIN006-1C US		09/849,005		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.				
(Use several sheets if necessary)								
				Filing Date		Group		
				MAY 4, 2001		2128		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	N
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	Factor, M., et al., "Rigorous Testing Using SnapShot", Israeli Conference on Computer Systems and Software Engineering, Herzliya, Israel, June 18-19, 1997, pp. 12-21.						
RF	AJ	Rundin, H., "Protocol Engineering: A Critical Assessment", Proceedings of the IFIP WG 6.1 Eighth International Symposium on Protocol Specification, Testing, and Verification Atlantic City, NJ, June 7-10, 1998, pp. 5-16.						
RF	AK	Stucki, L., et al., "New Assertion Concepts for Self-Metric Software Validation", International Conference on Reliable Software, Los Angeles, CA, April 21-23, 1975, pp. 59-71.						
RF	AL	Heimdahl, M., "Experiences and Lessons from the Analysis of TCAS II", Software Engineering Notes, Vol. 21, Number 3 (ISSTA), May 1996, pp. 79-83.						
RF	AM	Dou, C., "Integration of SDL and VHDL for HW/SW Codesign of Communication Systems", 23rd Euromicro Conference, Budapest, Hungary, September 1-4, 1997, pp. 188-195.						
RF	AN	Coen-Porisini, A., "Specification of Realtime Systems Using Astral", IEEE Transactions on Software Engineering, Vol. 23, No. 9, September 1997, pp. 572-598.						
RF	AO	Hamlet, R., "Theoretical Comparison of Testing Methods", Software Engineering Notes, Volume 14, No. 8, ACM SIGSOFT '89 Third Symposium on Software Testing Analysis, and Verification (TAV3), Key West, FL, December 13-15, 1989, pp. 28-37.						
Examiner		RUSSELL FRETZ		Date Considered		1.12.05		
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

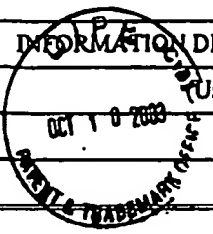
U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
				01N006-1C US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicants: Chian-Min Ho et al.			
(Use several sheets if necessary)							
				Filing Date		Group 2128	
				MAY 4, 2001		2128	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Denney, R., "Test-Case Generation from Prolog-Based Specifications", <u>Software Testing</u> , March 1991, pp. 49-57.					
RF	AJ	Monaco, J., "Functional Verification Methodology for the PowerPC 604™ Microprocessor", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 319-324.					
RF	AK	Luckham, D., et al., "An Event-Based Architecture Definition Language", IEEE Transactions on Software Engineering, Vol. 21, No. 9, September 1995, pp. 717-734.					
RF	AL	Rosenblum, D., "A Practical Approach to Programming With Assertions", IEEE Transactions on Software Engineering, Vol. 21, No. 1, January 1995, pp. 19-31.					
RF	AM	Ho, R., et al., "Architecture Validation for Processors", 22 <sup>nd</sup> Annual International Symposium on Computer Architecture, Santa Margherita Ligure, Italy, June 22-24, 1995, pp. 404-413.					
RF	AN	Goering, R., "Startup zeroes in on tough logic bugs in verification twist", Electronic Engineering Times, Monday June 1, 1998.					
RF	AO	Ho, R., et al., "Validation Coverage Analysis for Complex Digital Designs", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, Digest of Technical Papers, November 10-14, 1996, pp. 146-151.					
Examiner		Russell Freid		Date Considered		1.12.05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

U.S. Department of Commerce, Patent and Trademark Office						Atty. Docket No.		Serial No.	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						01N006-1C US		09/849,005	
						Applicants: Chian-Min Ho et al.			
						Filing Date		Group	
						MAY 4, 2001		2128	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Gburzynski, P. et al., "LANSE: A Protocol Modelling Environment and its Implementation", Software Practice and Experience Vol. 21(1), January 1991, pp. 51-76.							
RF	AJ	Crowley, J. L., et al., "Issues in the Full Scale Use of Formal Methods for Automated Testing", Software Engineering Notes, International Symposium on Software Testing and Analysis, San Diego, CA, January 8-10, 1996, pp. 71-78.							
RF	AK	Offutt, A. J., et al., "An Experimental Evaluation of Data Flow and Mutation Testing", Software-Practice and Experience, Vol. 26(2), February 1996, pp. 165-176.							
RF	AL	DeMillo, R. A., "An Extended Overview of the Mocha Software Testing Environment", Second Workshop on Software Testing, Verification, and Analysis, Banff, Canada, July 19-21, 1988, pp. 142-151.							
RF	AM	Clarke, E. M., et al., "Word Level Model Checking - Avoiding the Pentium FDIV Error", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 645-648.							
RF	AN	Bryant, R. E., "Bit-Level Analysis of an SRT Divider Circuit", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 661-665.							
RF	AO	Schneider, B., et al., "Software Development in a Hardware Simulation Environment", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 684-689.							
Examiner		RUSSELL FREJA		Date Considered		1.12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									



U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.		
				01N006-1CUS		09/849,005		
<div style="text-align: center;">  <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)</p> </div>				Applicants: Chian-Min Ho et al.				
				Filing Date		Group 2128		
				MAY 4, 2001		2123		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AI	Smith, D. J., "VHDL & Verilog Compared & Contrasted - Plus Modeled Example Written in VHDL, Verilog and C., 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 771-776.						
RF	AJ	Knapp, D., et al., "Behavioral Synthesis Methodology for HDL-Based Specification and Validation, 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA June 12-16, 1995, pp. 286-291.						
RF	AK	Tomita, M., et al., "Rectification of Multiple Logic Design Errors in Multiple Output Circuits", 32 <sup>nd</sup> Design Automation Conference, San Diego, CA, 1994 pp. 212-217.						
RF	AL	Kam, Timothy, et al., "Implicit State Minimization of Non-Deterministic FSM's", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 250-257.						
RF	AM	Bryant, R. E., et al., "Verification of Arithmetic Circuits with Binary Moment Diagrams", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 535-541.						
RF	AN	Ly, Tai, "Scheduling using Behavioral Templates", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 101-106.						
RF	AO	Grayson, B., et al., "Statistics on Concurrent Fault and Design Error Simulation", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 622-627.						
Examiner		RUSSELL FREID		Date Considered		1/12/05		
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

U.S. Department of Commerce, Patent and Trademark Office						Atty. Docket No.:		Serial No.:	
						OIN006-1 E US		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						Applicants: Chian-Min Ho et al.			
						Filing Date		Group	
						MAY 4, 2001		2128 2423	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Swamy, G., et al., "Incremental Methods for FSM Traversal", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 590-595.							
RF	AJ	Cyriluk, D. A., et al., "Theorem Proving: Not an Esoteric Diversion, but the Unifying Framework for Industrial Verification", International Conference on Computer Design: VLSI in Computers & Processors, Austin, TX, October 2-4, 1995, pp. 538-544.							
RF	AK	Swamy, G. M., et al., "Incremental Formal Design Verification", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 6-10, 1994, pp. 458-465.							
RF	AL	Butler, K. M., "Heuristics to Computer Variable Orderings for Efficient Manipulation of Ordered Binary Decision Diagrams", 28 <sup>th</sup> ACM/IEEE Design Automation Conference, San Francisco, CA, June 17-21, 1991, pp. 417-420.							
RF	AM	Rudnick, E. M., et al., "Sequential Circuit Test Generation in a Genetic Algorithm Framework", 31 <sup>st</sup> Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 698-704.							
RF	AN	Wing, J. M., "A Specifier's Introduction to Formal Methods", Computer, Vol. 23, No. 9, September 1990, pp. 8-24.							
RF	AO	Keen, J. "Specification for Duplo SNaC RLT Assertion Language", December 6, 1996.							
Examiner		RUSSELL FRETZ		Date Considered		1:12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				OIN 006-1C US		09/849,005		
				Applicants: Chian-Min Ho et al.				
				Filing Date		Group 2/28		
				MAY 4, 2001		-2123		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
RF	AJ	Golson, S., "State Machine Design Techniques for Verilog and VHDL", <a href="http://www.synopsys.com/pubs/JHLD/JHLD-099401">http://www.synopsys.com/pubs/JHLD/JHLD-099401</a> , believed to be prior to October 1997.						
RF	AJ	Schroeder, S., "Turning to Formal", Integrated System Design, September 1987, pp. 15-20.						
RF	AK	Panda, S., et al., "Symmetry Detection and Dynamic Variable Ordering of Decision Diagrams", IEEE/ACM International Conference on Computer-Aided Design, November 6-10, 1994, pp. 628-631.						
RF	AL	Iwashita, H., et al., "CTL Model Checking Based on Forward State Traversal", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 6-10, 1996, pp. 82-87.						
RF	AM	Hojati, R., et al., "Verification Using Uninterpreted Functions and Finite Instantiations" Formal Methods in Computer-Aided Design, First International Conference FMCAD '96, Palo Alto, CA November 6-8, 1996, pp. 218-233.						
RF	AN	Narayan, A., et al., "Partitioned ROBDDs - A Compact, Canonical and Efficiently Manipulable Representation for Boolean Functions", IEEE/ACM International Conference on Computer-Aided Design, November 6-10, 1996, pp. 547-554.						
RF	AO	Zhou, Z., "Formal Verification of the Island tunnel Controller Using Multiway Decision Graphs", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 218-232.						
Examiner		Russell F. Reid		Date Considered		1, 12, 05		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

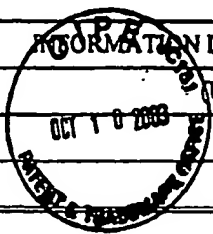
U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
<div style="position: relative; height: 100px;"> <div style="position: absolute; top: 0; left: 0; width: 100%; height: 100%; border: 1px solid black; border-radius: 50%; text-align: center; line-height: 100px; font-size: 24px; font-weight: bold;"> INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) </div> <div style="position: absolute; top: 10%; left: 10%; font-size: 12px;"> OCT 10 2003  PMTA - TRADEMARK </div> </div>				01N006-1C US		09/849,005	
				Applicants: Chian-Min Ho et al.			
				Filing Date		Group	
				MAY 4, 2001		2128 2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Lee, W., et al., "Tearing Based Automatic Abstraction for CTL Model Checking", San Jose, CA, November 10-14, 1996, pp. 76-81.					
RF	AJ	Ravi, Kavita, et al., "High-Density Reachability Analysis", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 5-9, 1995, pp. 154-158.					
RF	AK	Cho, H., et al., "A Structural Approach to State Space Decomposition for Approximate Reachability Analysis", IEEE International Conference on Computer Design: VLSI in Computers and Processors, Cambridge, MA, October 10-12, 1994, pp. 236-239.					
RF	AL	Cho, H., et al., "A State Space Decomposition Algorithm for Approximate FSM Traversal", IEEE, 1994, pp. 137-141.					
RF	AM	Cho, H., et al., "Algorithms for Approximate FSM Traversal", 30 <sup>th</sup> ACM/IEEE Design Automation Conference, 1993, pp. 25-30.					
RF	AN	Butler, R. W., et al., "The Infeasibility of Quantifying the Reliability of Life-Critical Real-Time Software" believed to be prior to 1997.					
RF	AO	Woods, S., et al., "Efficient Solution of Systems of Boolean Equations", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 10-14, 1996, pp. 542-546.					
Examiner		RUSSELL FREED		Date Considered		1.12.05	
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>							

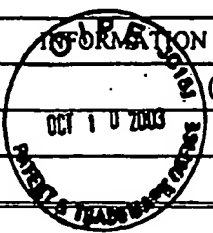
U.S. Department of Commerce, Patent and Trademark Office						Atty-Docket No.		Serial No.	
						OIN 006-1CUS		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)						Applicants: Chian-Min Ho et al.			
						Filing Date		Group	
						MAY 4, 2001		2123	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
	AC								
	AD								
	AE								
	AF								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AG								
	AH								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
RF	AI	Cabodi, G., et al., "Improved Reachability Analysis of Large Finite State Machines", IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, November 10-14, 1996, pp. 354-360.							
RF	AJ	Ganapathy, G., et al., "Hardware Emulation for Functional Verification of K5", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 315-318.							
RF	AK	Sawant, S., et al., "RTL Emulation: The Next Leap in System Verification", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 233-235.							
RF	AL	Daga, A. J., et al., "The Minimization and Decomposition of Interface State Machines", 31 <sup>st</sup> Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 120-125.							
RF	AM	Narayan, S., et al., "Interfacing Incompatible Protocols using Interface Process Generation", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 468-473.							
RF	AN	Monohan, Chuck, et al., "Symbolic Modeling and Evaluation of Data Paths", 32 <sup>nd</sup> Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 389-394.							
RF	AO	Marculescu, D., et al., "Stochastic Sequential Machine Synthesis Targeting Constrained Sequence Generation", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 696-701.							
Examiner		Russell FRETZ		Date Considered		1.12.05			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Serial No.	
				Q/N006-1C US		09/849,005	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (Use several sheets if necessary)				Applicants: Chian-Min Ho et al.			
				Filing Date		Group 2/28	
				MAY 4, 2001		-2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Verlind, E., et al., "Efficient Partial Enumeration for Timing Analysis of Asynchronous Systems", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 55-58.					
RF	AJ	Popescu, V. et al., "Innovative Verification Strategy Reduces Design Cycle Time For High-End SPARC Processor", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 311-314.					
RF	AK	Casaubieilh, F., et al., "Functional Verification Methodology of Chameleon Processor", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 421-426.					
RF	AL	Brown, S., et al., "Experience in Designing a Large-scale Multiprocessor using Field Programmable Devices and Advanced CAD Tools", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 427-432.					
RF	AM	Norris, C., "State Reduction Using Reversible Rules", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 564-567.					
RF	AN	Sanghavi, J., et al., "High Performance BDD Package By Exploiting Memory Hierarchy", 33 <sup>rd</sup> Design Automation Conference, Las Vegas, NV, 1996, pp. 635-640.					
RF	AO	Meyer, W., et al., "Design and Synthesis of Array Structured Telecommunication Processing Applications", 34 <sup>th</sup> Design Automation Conference, Anaheim, CA, June 9-13, 1997, pp. 486-491.					
Examiner		RUSSELL FREED		Date Considered		1. 12. 05	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

PART "B"

Sheet 23 of 24

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket N .		Serial No.	
				01N0061CUS		09/849,005	
				Applicants: Chian-Min Ho et al.			
				Filing Date		Group 2128	
				MAY 4, 2001		-2123	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
	AG						
	AH						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
RF	AI	Seawright, A., et al., "A System for Compiling and Debugging Structured Data Processing Controllers", EURO, Design Automation Conference, 1996.					
RF	AJ	Data Sheet "ATC's CoverMeter™ USA Commercial Price List, 1996.					
RF	AK	Dill, D. L., et al., "Acceptance of Formal Methods: Lessons From Hardware Design", Computer, April 1996, pp. 23-24.					
RF	AL	Bullis, D., "Verification and Modeling for Synthesis-Based Design", Marketing Communications, believed to be prior to 1997, pp. 15-17.					
RF	AM	Article "Product expectations in networking have risen to a point where systems must be self-correcting. The added cost of 'safe' design practices is not even questioned", Electronic Engineering Times, November 11, 1996, p. 48.					
RF	AN	Young, L. H., "Building A Better Bug Trap", Electronic Business Today, November 1996, pp. 49-53.					
RF	AO	Silbey, A. "The Systems Challenge for EDA Tools" Viewlogic Systems, believed to be prior to October 1997, pp. 22-26.					
Examiner		Russell FRETZ		Date Considered		1.12.05	
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>							

U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Serial No.		
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				01N0061C US		09/849,005		
				Applicants: Chian-Min Ho et al.				
				Filing Date		Group 2128		
				MAY 4, 2001		-2123-		
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
	AF							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
21	AI	Singer, S., et al., "Next Generation Test Generator (NGTG) for Digital Circuits", AUTOTESTCON, 97, 1997 IEEE Autotestcon Proceedings, Septe. 22-25, 1997, pp. 105-112.						
	AJ							
	AK							
	AL							
	AM							
	AN							
	AO							
Examiner		Russell FRETZ		Date Considered		1.12.05		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								